



VICAM[®] III

Digital Imaging Engine Product Specification Revision 2.5

TABLE OF CONTENTS

1	Introduction	3
1.1	Related Documents	3
2	ViCAM [®] III Digital Imaging Engine General Description.....	3
2.1	ViCAM [®] III Main Features.....	3
2.2	ViCAM [®] III Performance Factors.....	4
3	ViCAM [®] III ASIC Block Diagram.....	5
4	ViCAM [®] III Pin Specifications	6
5	ViCAM [®] III Electrical Specifications	9
6	ViCAM [®] III Package Information	11
7	ViCAM [®] III Soldering Reflow Instructions	14
8	ViCAM [®] III Ordering Information	15

1 Introduction

This document presents product specifications of the ViCAM[®] III Digital Imaging Engine ASIC's. This document should be read in conjunction with the related documents defined below.

1.1 Related Documents

ViCAM[®] III Overview (ViCAMIIIOverview document)

ViCAM[®] III Register Map (ViCAMIIIRegMap document)

ViCAM[®] III Processor Instruction Set Definition (ViCAMIII_pg document)

2 ViCAM[®] III Digital Imaging Engine General Description

The ViCAM[®] III provides an intelligent and programmable digital video signal processing engine that is powerful enough to allow for a stand alone digital camera, yet flexible enough to allow it to interface to nearly any transport (communication) interface that may be required. The ViCAM[®] III Digital Imaging Engine has been designed to allow a rapid and economical implementation of a broad range of products such as a USB camera (USB 1.1), Serial port camera (RS232), Wireless Camera (802.11), NetCam (Ethernet or modem), a dual-mode camera (portable WebCam), a Digital Still Camera, Digital Video Recorders, and many more.

2.1 ViCAM[®] III Main Features

The major features of ViCAM[®] III include:

- Supports CCD or CMOS image sensors with RGB or CMYG color filters. Support for any sensor resolution up to 4k pixels per line. Supports both interlaced and progressive scan sensors.
- Programmable Image data path providing a full range of image controls (gamma, sharpness, color matrix, contrast, etc..)
- Digital Video input port. Provides support for composite video front end input (digital YUV input bus), for existing off the shelf components from Techwell, Philips, Conexant (Brooktree), etc...
- YUV 4:2:2 video data output port support for ZV port or CCIR601 data stream. Can provide digital video at full resolution / full frame rates, (e.g. Frame rate up to 30 frames per second at 640 x 480).
- On-chip hardware based programmable JPEG video compression/decompression engine.
- On chip 50MIPs programmable VII micro-controller (performance based on clock speed). Powerful enough for most camera product implementations
- Implements internal or host based control loops (i.e. AGC, White balance).
- On-chip multi end-point USB Controller.
- Programmable CCD/CMOS signal timing generator.
- User selectable scan rates and shutter time.

- Support for external or internal asynchronous frame acquisition.
- Processor address/data port provides expansion capability and processor access to external logic such as a parallel port, Fire-Wire, DSP based modem, Ethernet or TCP/IP engine, Security/Encryption chips, RAM/ROM memory, Compact Flash, IDE drives, etc....
- On-chip UART, (polled or interrupt driven)
- Serial Peripheral Interface (SPI) controllers with 4 chip selects.
- Support for Digital Audio I/O via on-chip multiple mode Audio Codec interface port.
- Hardware based digital zoom and pan (area of interest read-out).
- Support for pan, tilt, zoom, electronic iris, flash, and auto focus hardware via programmable I/O.
- Camera firmware can be stored in local EEPROM or downloadable by host.
- Versatile frame buffer memory controller supports SDRAM or SSRAM, allowing the memory size and type to be optimised for the product requirements.
- Available in three packages, a 256 pin BGA package full featured version, a 208 pin BGA package semi-full featured version with reduced size, and a 144 pin BGA package providing functionality for low cost WebCam tethered product applications in our smallest size.

2.2 ViCAM[®] III Performance Factors

The ViCAM[®] III contains a pipelined datapath able to process input pixel data at up to 20 mega-pixels per second coupled with a frame buffer interface that operates at over 100 megabytes per second. Combined with the JPEG codec which can operate at 40 mega-pixels per second enables a ViCAM[®] III camera to generate full frame rate video at full resolution (i.e. 640 x 480 @ 30FPS) over a standard USB port. The on-chip image scaler and compression engine will allow slower interfaces to support full speed video at lower quality settings. The on-chip microprocessor runs firmware that implements the camera command interface (ViCAM[®] III API) and internal control algorithms such as AGC and AWB. Baseline USB camera firmware uses less than 25% of the available processor bandwidth. This allows for significant processing power available for application specific firmware or the processor can be clocked slower to reduce power consumption.

3 ViCAM[®] III ASIC Block Diagram

Presented below is a block diagram of the complete ViCAM[®] III Digital Imaging Engine showing the different sections of the ASIC. Please refer to the “Related Documents” section for detailed information on the ViCAM[®] III Digital Imaging Engine’s functional blocks and sections.

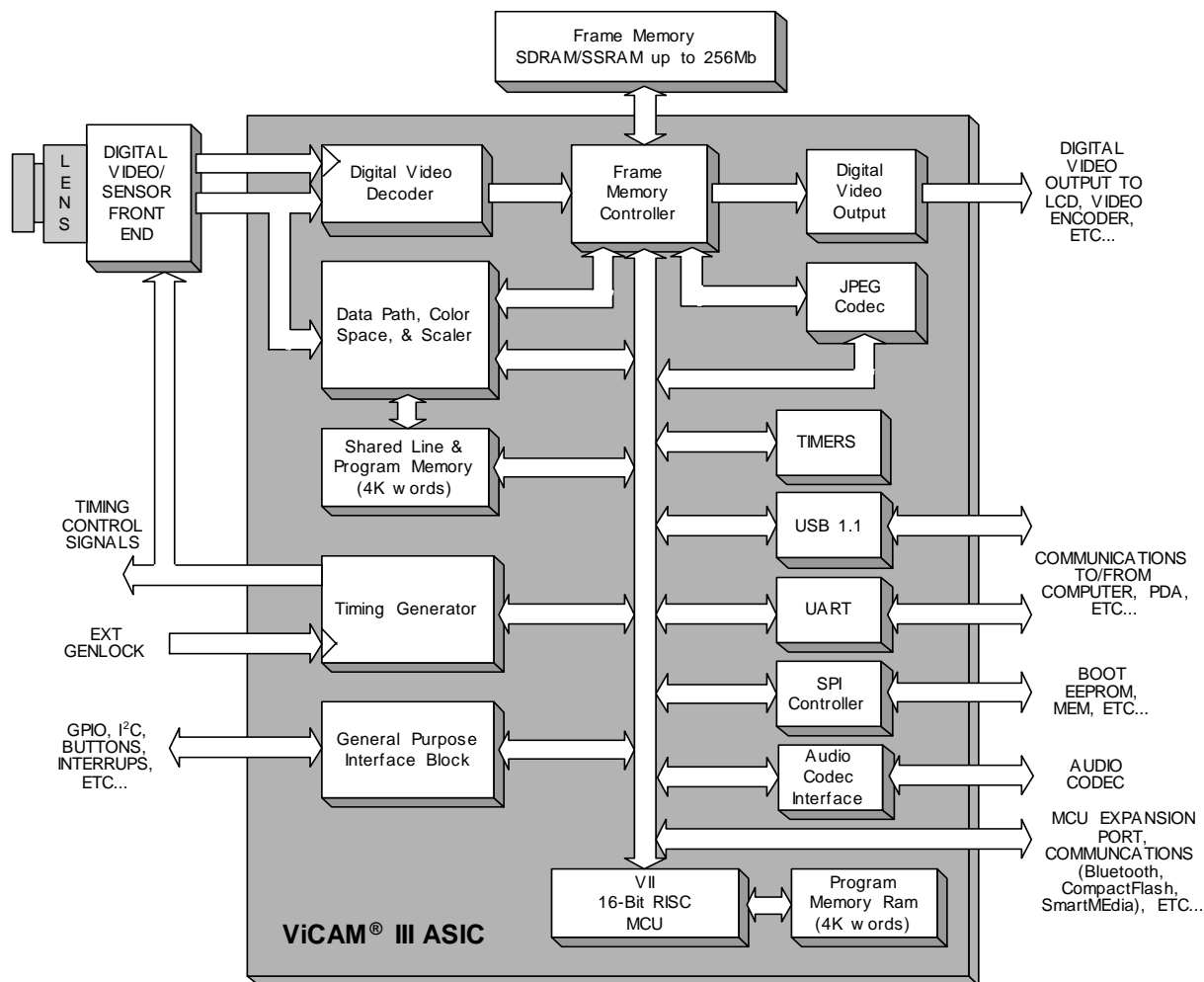


Figure 3-1 ViCAM[®] III ASIC Block Diagram

4 ViCAM[®] III Pin Specifications

This section presents the details of the ViCAM[®] III Digital Imaging Engine's pin out and signal definition.

Pin Name	BGA256 Pins	BGA208 Pins	BGA144 Pins	Description
Digital Sensor/Video Input Port Signals				
VDI[0] - [9]	H1, J2, K2, L2, M1, N1, P1, R1, R2, R3	F1, G3, H2, H3, J1, K2, K3, L1, M2, M1	E2, F3, F1, F2, G1, H3, G2, H1, H2, J3	Digital Video Input Data [0 - 9] - Can be Digital Sensor Data or Digital Video Data (discrete signal or CCIR601 modes)
VICLK	E1	F3	D3	Digital Video Input Port Clock - used as pixel clock to ASIC when in digital video mode
VIVLD	G2	F2	E3	Digital Video Input Port Data Valid Signal - used as data valid indicator when in discrete signal digital video mode
VIFLD	G1	G4	E1	Digital Video Input Port Field Signal - used as field indicator when in discrete signal digital video mode
VIHS	G3	E1	D1	Digital Video Input Port Horizontal Sync Signal - used as horizontal sync signal when in discrete signal digital video mode
Digital Video Output Port Signals				
VOS[0] - [7]	E3, B1, D2, D1, F2, F1, H3, H2	B2, B1, D2, E2 (V0S4-7 N/A)	N/A	Digital Video Output Port Control Signals - Programmable timing and control signals which are customized for the specific interface of the digital video output port
VDO[0] - [15]	J3, J1, K1, L1, M2, N2, P2, P3, T1, T2, U3, W2, AA1, W3, Y5, AB2	G2, G1, H1, J2, J3, K1, L2, L3 (VDO8-15 N/A)	N/A	Digital Video Output Port Data [0 - 15] - Configurable to multiplexed 8bit, 16bit, or CCIR601 data formats
External Processor Port Signals				
PADDR[0] - [15]	AA4, AB4, AB5, Y7, AA7, AB7, AB8, AA9, AA11, AB12, AB13, AB14, AB15, AA15, Y15, AB17	T2, R5, U2, U4, T4, T5, U6, U7, R9, U9, R10, T10, U11, R11, T12, R12	N/A	External Processor Port Address [0 - 15] - Used for accessing external hardware and/or monitoring the processor activity while in debug mode
PDATA[0] - [15]	L22, K22, J22, H22, H21, H20, F22, G20 C19, B20, C17, A20, B18, B17, A17, C15	K17, J16, J15, H17, G16, F17, G15, E16, B16, C14, A16, B14, C12, B13, C11, A11	N/A	External Processor Port Data [0 - 15] - Used for accessing external hardware and/or monitoring the processor activity while in debug mode
READ-	Y16	R13	N/A	External Processor Port Read Strobe Signal
WRITE-	AB18	U14	N/A	External Processor Port Write Strobe Signal
WAIT	AA18	U15	N/A	External Processor Port Wait Signal - used by external devices to wait state the processor during access
EXTCS[1] - [4]	D21, B22, A15, B14	E15, D15, A10, C9	N/A	External Chip Select [1 - 4] - Configurable device select signals
DOP	B3	N/A	N/A	Debug OpCode State Signal - When in debug mode can be used as a qualifying signal to detect when the processor's access is an opcode fetch operation
DRD	A3	N/A	N/A	Debug Read State Signal - When in debug mode can be used as a qualifying signal to detect when the processor's access is a read operation

Pin Name	BGA256 Pins	BGA208 Pins	BGA144 Pins	Description
DWR	C5	N/A	N/A	Debug Write State Signal - When in debug mode can be used as a qualifying signal to detect when the processor's access is a write operation
Frame Memory Signals				
FADDR[0] - [13]	W20, Y21, U20, Y22, V21, U21, U22, R20, T22, R21, P20, P22, N22, M21	T17, P15, P16, N15, P17, N16, N17, M16, M15, M17, L14, L16, L15, L17	M12, L12, N13, M13, L13, K12, K13, J13, J12, J11, H13, H12, H11, G13	Frame Memory Address [0 - 13]
FADDR[14] - [23]	V20, AA22, W21, W22, V22, T20, T21, R22, P21, N21	R16, R17 (FADDR16-23 N/A)	N/A	Frame Memory Address [14 - 23]
FDATA[0] - [15]	M22, L21, K21, J21, J20, G22, G21, F21, C18, A21, B19, A19, A18, C16, B16, A16	K16, K15, J17, H16, H15, G17, F16, E17, B15, A15, C13, A14, A13, A12, B12, C10	G12, F13, F12, F11, E13, E11, E12, D13, A13, B11, A12, A11, B10, A10, C10, B9	Frame Memory Data [0 - 15]
FM_CS-	E20	A17	B13	Frame Memory Chip Select
FM_CKE	C21	C16	C12	Frame Memory Clock Enable
FM_CAS-	E21	C17	C13	Frame Memory Column Address Strobe
FM_RAS-	E22	F15	D11	Frame Memory Row Address Strobe
FM_WR-	C22	B17	D12	Frame Memory Write
General Purpose I/O [0-10] Signals				
GPIO[0] - [10]	A10, A9, A8, B8, C8, A6, C7, A4, B4, A2, C4	A7, B7, A6, D7, A5, B5, A4, B4, B3, C4, A1	A7, C6, A6, B6, C5, B5, A4, C4, B3, A2, B2	General Purpose I/O [0 - 10]
General Purpose I/O [11-15] & Audio Codec Interface Signals				
GPIO[11]	D3	D3	A1	General Purpose I/O [11] & Audio Codec Interface TXD Signal
GPIO[12]	C2	C2	B1	General Purpose I/O [12] & Audio Codec Interface RXD Signal
GPIO[13]	F3	C1	C2	General Purpose I/O [13] & Audio Codec Interface SYNC Signal
GPIO[14]	C1	E3	C1	General Purpose I/O [14] & Audio Codec Interface SCLK Signal
GPIO[15]	E2	D1	D2	General Purpose I/O [15] & Audio Codec Interface MCLK Signal
Test Signals				
TDI	B10	N/A	N/A	JTAG Data In
TDO	A11	N/A	N/A	JTAG Data Out
TRST	A7	N/A	N/A	JTAG Reset
TCLK	B9	N/A	N/A	JTAG Clock
TMS	C9	N/A	N/A	JTAG Mode Select
TEST[1] - [3]	AB16, AA16, AA17	U12, U13, T13	N9, L9, M9	Test Modes [1,2,3] 3=0, 2=0, 1=0 - Normal Mode 3=0, 2=0, 1=1 - MBIST Test Mode 3=0, 2=1, 1=0 - JTAG Test Mode 3=1, 2=1, 1=1 - SCAN Test Mode
Clock Related Signals				
MCLKI	Y17	R14	N10	Main Clock Input
MCLKO	AB20	T15	M10	Main Clock Output
MXIN	AA19	U17	L10	Main Crystal Oscillator Input
MXOUT	Y18	U16	N11	Main Oscillator Out
UXIN	AB21	T16	M11	USB 48 Mhz Crystal Oscillator Input
UXOUT	AA20	R15	N12	USB Oscillator Out
CLKDLYI	AA14	P11	M8	Delayed Clock In
CLKDLYO	AA13	U10	N8	Delayed Clock Out

Pin Name	BGA256 Pins	BGA208 Pins	BGA144 Pins	Description
Misc Signals				
SUSPEND	AA12	T9	N7	Suspend Output to put external H/W in standby (Active High)
RESUME	D20	C15	B12	Resume from Standby Input
INT[0] - [2]	AB19, D22, F20	T14, D17, D16	N/A	External Interrupt Input [0 - 2]
BUT[0] - [1]	B5, C6	A3, A2	B4, A3	Button Input [0 - 1]
NRST	Y14	T11	L8	Chip Reset - Low true
Power Supply Signals				
VCC2V	D18, D5, E19, E4, V19, V4, W18, W5	D8, D10, D11, H4, H14, K4, K14, P7, P8, P10	C11, C3, D10, D4, K10, K4, L11, L3	Core Power 2.5VDC
VCC3V	C10, C11, C12, C13, K20, K3, L20, L3, M20, M3, N20, N3, Y10, Y11, Y12, Y13	D6, D12, F4, F14, G14, L4, M4, M14, P6, P12	C7, D7, G10, G11, G3, G4, K7, L7	I/O Power 3.3VDC
VSS	A1, A22, AA2, AA21, AB1, AB22, B2, B21, C20, C3, D19, D4, K10, K11, K12, K13, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, W19, W4, Y20, Y3	C3, D4, D5, D9, D13, D14, E4, E14, J4, J14, N4, N14, P4, P5, P9, P13, P14	D5, D6, D8, D9, E10, E4, F10, F4, H10, H4, J10, J4, K5, K6, K8, K9	Signal/Pwr Gnd
SPI Bus Signals				
SCS0	A13	C8	A8	SPI Boot Rom Chip Select Signal
SCLK	C14	B10	C9	SPI Boot Rom Clock Signal
SDI	B15	B11	A9	SPI Boot Rom Data Input Signal
SDO	A14	A9	B8	SPI Boot Rom Data Output Signal
SCS1	B7	B6	A5	SPI Bus Chip Select 1
SCS[2] - [3]	B6, A5	C6, C5	N/A	SPI Bus Chip Selects [2 - 3]
Timing Generator Signals				
TG[0] - [19]	U1, U2, T3, V1, W1, V2, Y1, V3, Y2, Y4, AA3, Y6, AB3, AA5, AA6, AB6, Y8, AA8, Y9, AB9	N2, M3, N1, P2, P1, N3, R1, T1, P3, R4, R3, R2, U1, T3, U3, R6, U5, R7, T6, R8	J1, K3, J2, K1, L1, K2, M3, M1, L2, M2, N1, N2, N3, M4, M5, N4, L4, N5, L5, M6	Timing Generator Outputs [0 - 19]
UART I/O Signals				
RXD	A12	B8	C8	UART Receive Data Signal
TXD	B11	C7	B7	UART Transmit Data Signal
RTS	B13	B9	N/A	UART Request To Send
CTS	B12	A8	N/A	UART Clear To Send
USB I/O Signals				
USBDM	AB10	U8	L6	USB Data -
USBDP	AA10	T7	N6	USB Data +
USBPU	AB11	T8	M7	USB Port Pullup
No Connect Pins				
	Y19	N/A	K11	

5 ViCAM[®] III Electrical Specifications

ViCAM[®] III Digital Imaging Engine's electrical information for both the BGA256 and BGA144 packages.

Absolute Maximum Ratings (1)

SYMBOL	PARAMETER	RATING	UNITS
V _{CC}	2.5V Power Supply	-0.3 to 3.0	V
	3.3V Power Supply	-0.3 to 3.9	V
V _{IN2}	Input Voltage of 2.5V I/O	-0.3 to V _{CC2I} + 0.3	V
V _{IN3}	Input Voltage of 3.3V I/O with 5V Tolerance	-0.3 to 5.5	V
T _{STG}	Storage Temperature	-40 to 150	°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{CCK}	Core Power Supply	2.25	2.5	2.75	V
V _{CC3O}	Power Supply of 3.3V I/O	3.0	3.3	3.6	V
V _{IN2}	Input Voltage of 2.5V I/O	0	2.5	2.75	V
V _{IN3} T _j	Input Voltage of 3.3V I/O with 5V Tolerance	0	3.3	5.25	V
	Commercial Junction Operating Temperature	0	25	115	°C
	Industrial Junction Operating Temperature	-40	25	125	°C

Leakage Current and Capacitance (3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I _{IL}	Input Leakage Current (2)	No pull-up or pull-down	-10		10	μA
I _{oZ}	Tri-state Leakage Current		-10		10	μA
C _{IN2}	Input Capacitance (3)			3.1		pF
C _{OUT2}	Output Capacitance (3)			3.1		pF
C _{BID2}	Bi-directional Buffer Capacitance (3)			3.1		pF

- (1). Permanent device damage may occur if Absolute Maximum Rating are exceeded.
- (2). The pull up/pull down input leakage current can be derived from the pull up/pull down resistance (R_{pu}/R_{pd}) in the DC characteristics table for each type I/O buffer.
- (3). The capacitances listed above do not include PAD capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance's which is about 0.1 pF and the package capacitance.

DC Characteristics of True 2.5V I/O Cells (U_{Xin}, U_{Xout}, M_{Xin}, M_{Xout})

(under Recommended Operating Conditions, T_j = 0°C to +115°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{CCK}	Core Power Supply	Core Area	2.25	2.5	2.75	V
V _{CC2I}	Power Supply	2.5V I/O	2.25	2.5	2.75	V
V _{CC2O}	Power Supply		2.25	2.5	2.75	V
V _{IL}	Input Low Voltage	CMOS			0.3*V _{CC}	V
V _{IH}	Input High Voltage	CMOS	0.7*V _{CC}			V
V _t	Switching Threshold	CMOS		1.2		V
V _{t-}	Schmitt Trigger Negative Going Threshold Voltage	CMOS	0.7	1.0		V
V _{t+}	Schmitt Trigger Positive Going Threshold Voltage	CMOS		1.5	1.7	V
V _{OL}	Output Low Voltage	I _{OL} =2,4,.....,16 mA			0.4	V
V _{OH}	Output High Voltage	I _{OH} =2,4,.....,16 mA	1.85			V

R _{pu} /R _{pd}	Input Pull-up/Pull-down Resistance		40	75	190	KΩ
I _{IN}	Input Leakage Current	V _{in} =0 or VCC2I	-10		10	μA
I _{oZ}	Tri-state Leakage Current		-10		10	μA

DC Characteristics of True 3.3V I/O Cells (USBDP, USBDN)

 (under Recommended Operating Conditions, T_j = 0°C to +115°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{CCK}	Core Power Supply	Core Area	2.25	2.5	2.75	V
V _{CC3I}	Power Supply	3.3V I/O	3.0	3.3	3.6	V
V _{CC3O}	Power Supply		3.0	3.6	3.6	V
V _{IL}	Input Low Voltage *	CMOS/LVTTL			0.8	V
V _{IH}	Input High Voltage *	CMOS/LVTTL	2.0			V
V _t	Switching Threshold	CMOS/LVTTL		1.5		V
V _{t-}	Schmitt Trigger Negative Going Threshold Voltage	CMOS/LVTTL	0.8	1.1		V
V _{t+}	Schmitt Trigger Positive Going Threshold Voltage	CMOS/LVTTL		1.6	2.0	V
V _{OL}	Output Low Voltage	I _{OL} =2,4,.....,16 mA			0.4	V
V _{OH}	Output High Voltage	I _{OH} =2,4,.....,16 mA	2.4			V
R _{pu} /R _{pd}	Input Pull-up/Pull-down Resistance		40	75	190	KΩ
I _{IN}	Input Leakage Current	V _{in} =0 or VCC3I	-10		10	μA
I _{oZ}	Tri-state Output Leakage Current		-10		10	μA

* The input level is CMOS and LVTTL compatible. The V_{il(max)} = 0.3V_{CC} of CMOS also complied with the V_{il(max)} = 0.8 for LVTTL spec. The V_{ih(min)} = 2V of LVTTL also complied with the V_{ih(min)} = 0.7*V_{CC}

DC Characteristics of 5V Tolerant 3.3V Programmable I/O Cells

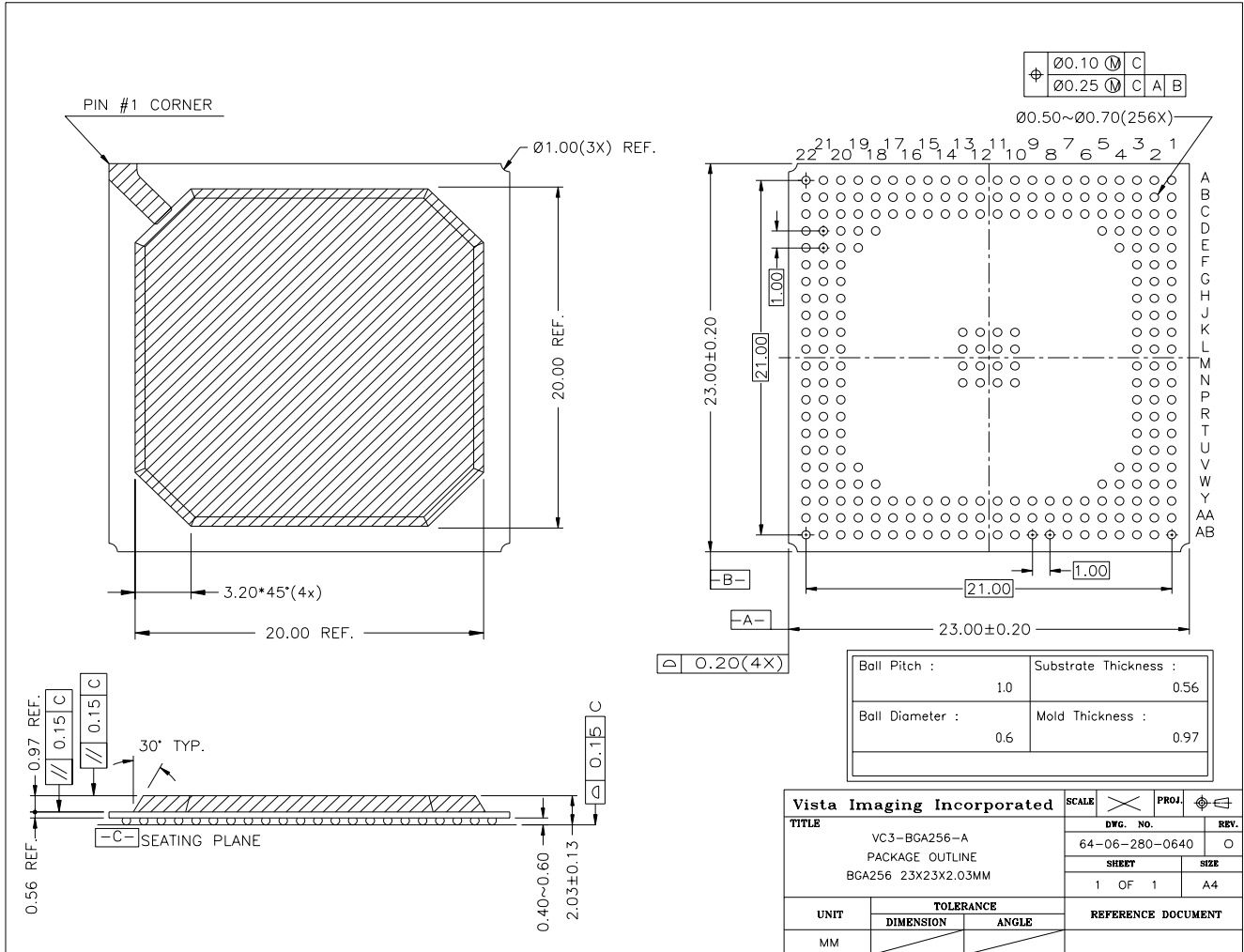
 (under Recommended Operating Conditions, T_j = 0°C to +115°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{CCK}	Core Power Supply	Core Area	2.25	2.5	2.75	V
V _{CC3I}	Power Supply	3.3V I/O	3.0	3.3	3.6	V
V _{CC3O}	Power Supply		3.0	3.3	3.6	V
V _{IL}	Input Low Voltage	PCI	-0.5		0.3*V _{cc}	V
V _{IH}	Input High Voltage		0.5*V _{cc}		5.5	V
V _t	Switching Threshold	PCI		1.3		V
V _{OL}	Output Low Voltage	I _{OUT} = 1.5 mA			0.1*V _{cc}	V
V _{OH}	Output High Voltage	I _{OUT} = 0.5 mA	0.9*V _{cc}			V
R _{pu} /R _{pd}	Input Pull-up/Pull-down Resistance		40	75	190	KΩ
I _{IN}	Input Leakage Current	V _{in} =0 or VCC3I	-10		10	μA
I _{oZ}	Tri-state Output Leakage Current		-10		10	μA

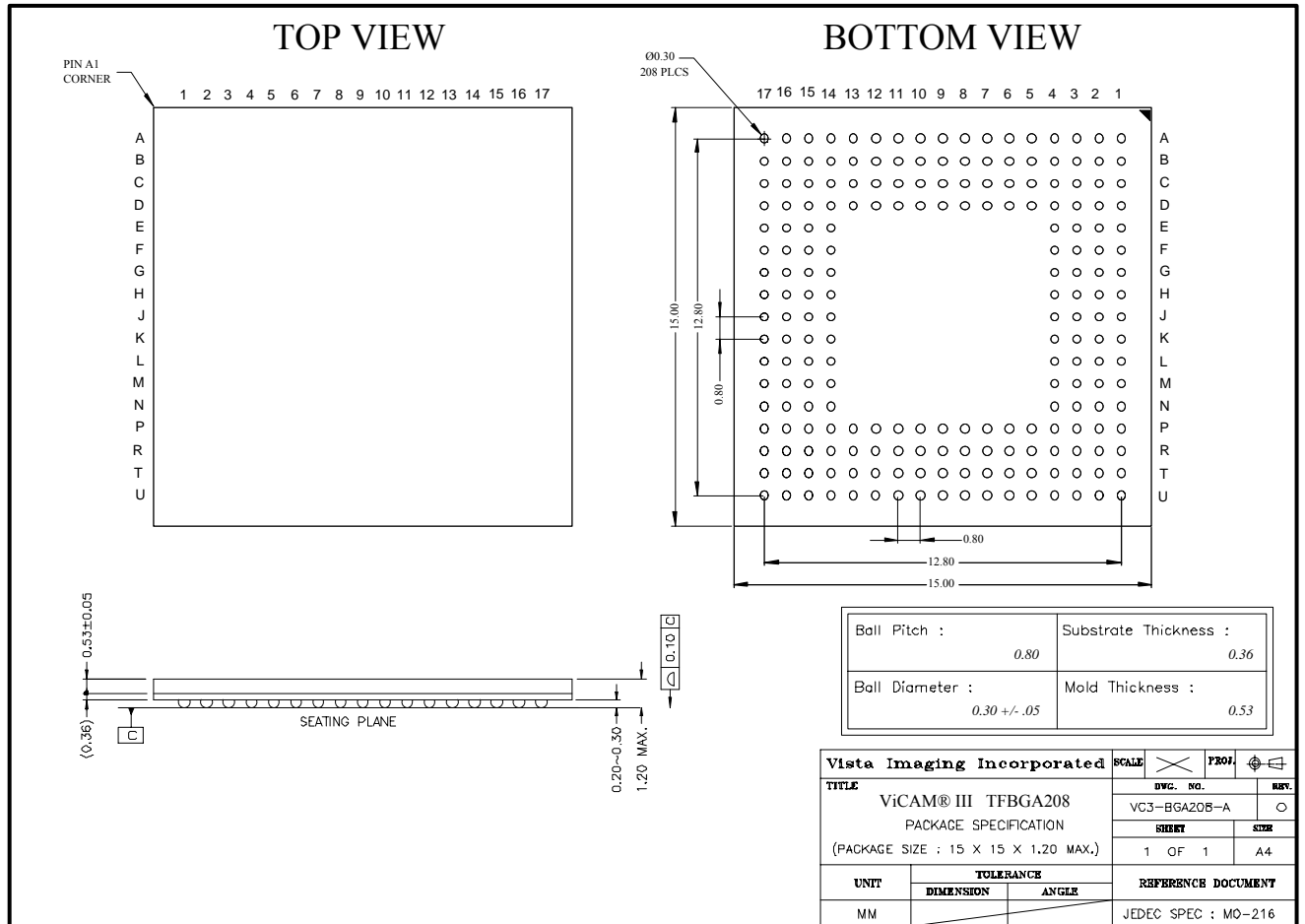
Vista Imaging assumes no responsibility for usage beyond the conditions within this specification.

6 ViCAM[®] III Package Information

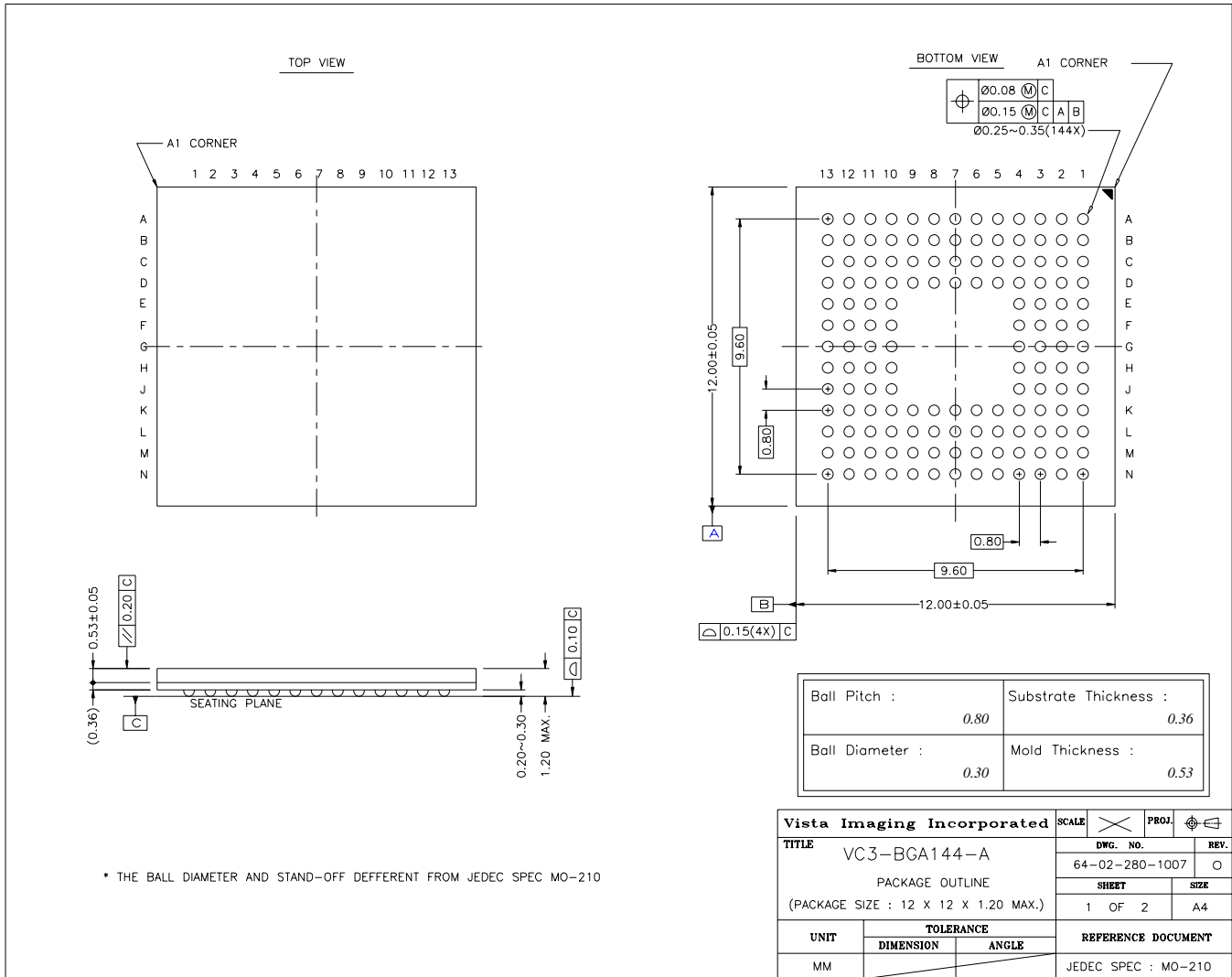
This section presents the details of the ViCAM[®] III Digital Imaging Engine's package information for the BGA256, BGA208, and BGA144 packages.



VC3-B256-A Package Drawing



VC3-B208-A Package Drawing



VC3-B144-A Package Drawing

7 ViCAM[®] III Soldering Reflow Instructions

Package Reflow Condition:

Convection 220 +5/-0 °C

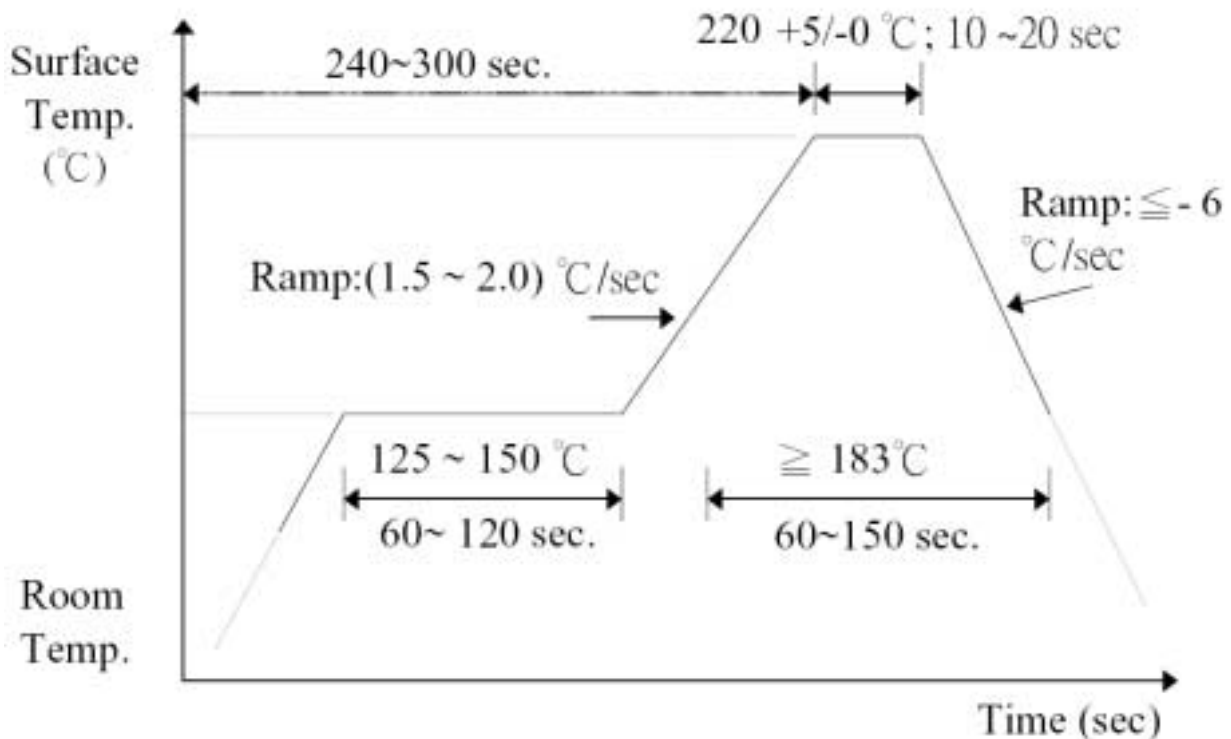
VPR 215~ 219 °C

IR / Convection 220 +5/-0 °C

Reflow Profile:

	Convection or IR / Convection	VPR
Average ramp-up rate (183 °C to Peak)	3 °C / second max.	10 °C / second max.
Preheat temp 125 (+25) °C	120 seconds max.	
Temp maintained above 183 °C	60 ~ 150 seconds	
Time within 5 °C of actual peak temp	10 ~ 20 seconds	60 seconds
Peak temperature range	220 +5 / -0 °C	215 ~ 219 °C
Ramp-down rate	6 °C / second max.	10 °C / second max.
Time 25 °C to peak temp	6 minutes max.	

Note: All temperatures refer to the top side of the package, measured on the package body surface. The devices shall be allowed to cool down for five minutes minimum between Convection, IR/Convection, or VPR cycles.



8 ViCAM[®] III Ordering Information

Part Number	Package
VC3-B144-A	144 pin BGA (12mm x 12mm)
VC3-B208-A	208 pin BGA (15mm x 15mm)
VC3-B256-A	256 pin BGA (22mm x 22mm)

Vista Imaging Incorporated
521 Taylor Way
San Carlos, CA 94070 USA
Tel: (650) 802-9685
Fax: (650) 802-0322
Internet: www.vistaimaging.com