



# **VICAM<sup>®</sup> III**

## **Digital Imaging Engine Product Specification Revision 2.6**

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## **1 Introduction**

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This document presents product specifications of the ViCAM<sup>®</sup> III Digital Imaging Engine ASIC's. This document should be read in conjunction with the related documents defined below.

### **1.1 Related Documents**

ViCAM<sup>®</sup> III Overview (ViCAMIIIOverview document)

ViCAM<sup>®</sup> III Register Map (ViCAMIIIRegMap document)

ViCAM<sup>®</sup> III Processor Instruction Set Definition (ViCAMIII\_pg document) & programmers guide

## **2 ViCAM<sup>®</sup> III Digital Imaging Engine General Description**

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The ViCAM<sup>®</sup> III provides an intelligent and programmable digital video signal processing engine that is powerful enough to allow for a stand alone digital camera, yet flexible enough to allow it to interface to nearly any transport (communication) interface that may be required. The ViCAM<sup>®</sup> III Digital Imaging Engine has been designed to allow a rapid and economical implementation of a broad range of products such as a USB camera (USB 1.1), Serial port camera (RS232), Wireless Camera (802.11), NetCam (Ethernet or modem), a dual-mode camera (portable WebCam), a Digital Still Camera, Digital Video Recorders, and many more.

### **2.1 ViCAM<sup>®</sup> III Main Features**

The major features of ViCAM<sup>®</sup> III include:

- Supports CCD or CMOS image sensors with RGB or CMYG color filters. Support for any sensor resolution up to 4k pixels per line. Supports both interlaced and progressive scan sensors.
- Programmable Image data path providing a full range of image controls (gamma, sharpness, color matrix, contrast, etc..)
- Digital Video input port. Provides support for composite video front end input (digital YUV input bus), for existing off the shelf components from Techwell, Philips, Conexant (Brooktree), etc...
- YUV 4:2:2 video data output port support for ZV port or CCIR601 data stream. Can provide digital video at full resolution / full frame rates, (e.g. Frame rate up to 30 frames per second at 640 x 480).
- On-chip hardware based programmable JPEG/MJPEG video compression/decompression engine.
- On chip 50MIPs programmable VII micro-controller (performance based on clock speed). Powerful enough for most camera product implementations
- Implements internal or host based control loops (i.e. AGC, White balance).
- On-chip multi end-point USB Controller.
- Programmable CCD/CMOS signal timing generator.
- User selectable scan rates and shutter time.

- Support for external or internal asynchronous frame acquisition.
- Processor address/data port provides expansion capability and processor access to external logic such as a parallel port, Fire-Wire, DSP based modem, Ethernet or TCP/IP engine, Security/Encryption chips, RAM/ROM memory, Compact Flash, IDE drives, etc....
- On-chip UART, (polled or interrupt driven)
- Serial Peripheral Interface (SPI) controllers with 4 chip selects.
- Support for Digital Audio I/O via on-chip multiple mode Audio Codec interface port.
- Hardware based digital zoom and pan (area of interest read-out).
- Support for pan, tilt, zoom, electronic iris, flash, and auto focus hardware via programmable I/O.
- Camera firmware can be stored in local EEPROM or downloadable by host.
- Versatile frame buffer memory controller supports SDRAM or SSRAM, allowing the memory size and type to be optimised for the product requirements.
- Available in fully RoHS 208 pin BGA package.

## **2.2 ViCAM<sup>®</sup> III Performance Factors**

The ViCAM<sup>®</sup> III contains a pipelined datapath able to process input pixel data at up to 20 mega-pixels per second coupled with a frame buffer interface that operates at over 100 megabytes per second. Combined with the JPEG codec which can operate at 40 mega-pixels per second enables a ViCAM<sup>®</sup> III camera to generate full frame rate video at full resolution (i.e. 640 x 480 @ 30FPS) over a standard USB port. The on-chip image scaler and compression engine will allow slower interfaces to support full speed video at lower quality settings. The on-chip microprocessor runs firmware that implements the camera command interface (ViCAM<sup>®</sup> III API) and internal control algorithms such as AGC and AWB. Baseline USB camera firmware uses less than 25% of the available processor bandwidth. This allows for significant processing power available for application specific firmware or the processor can be clocked slower to reduce power consumption.

### 3 ViCAM<sup>®</sup> III ASIC Block Diagram

Presented below is a block diagram of the complete ViCAM<sup>®</sup> III Digital Imaging Engine showing the different sections of the ASIC. Please refer to the “Related Documents” section for detailed information on the ViCAM<sup>®</sup> III Digital Imaging Engine’s functional blocks and sections.

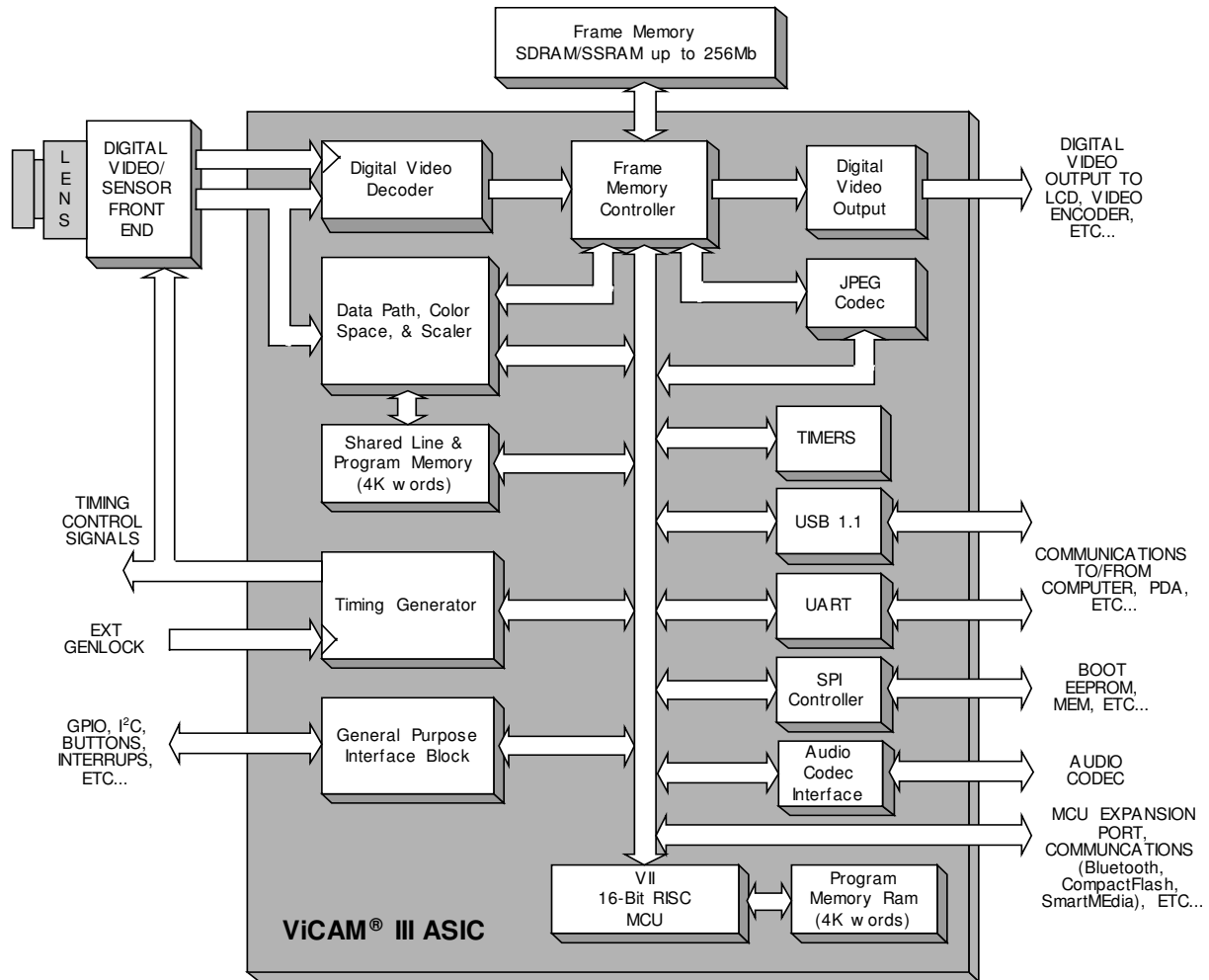


Figure 3-1 ViCAM<sup>®</sup> III ASIC Block Diagram

### 4 ViCAM<sup>®</sup> III Pin Specifications

This section presents the details of the ViCAM<sup>®</sup> III Digital Imaging Engine's pin out and signal definition.

| Pin Name         | BGA208 Pins  | Description  |
|------------------|--|--|
| VDI[0] - [9]     | F1, G3, H2, H3, J1, K2, K3, L1, M2, M1   | Digital Video Input Data [0 - 9] - Can be Digital Sensor Data or Digital Video Data (discrete signal or CCIR601 modes)   |
| VICLK            | F3   | Digital Video Input Port Clock - used as pixel clock to ASIC when in digital video mode  |
| VIVLD            | F2   | Digital Video Input Port Data Valid Signal - used as data valid indicator when in discrete signal digital video mode   |
| VIFLD            | G4   | Digital Video Input Port Field Signal - used as field indicator when in discrete signal digital video mode   |
| VIHS             | E1   | Digital Video Input Port Horizontal Sync Signal - used as horizontal sync signal when in discrete signal digital video mode  |
| VOS[0] - [7]     | B2, B1, D2, E2<br>(VOS4-7 N/A)   | Digital Video Output Port Control Signals - Programmable timing and control signals which are customized for the specific interface of the digital video output port |
| VDO[0] - [7]     | G2, G1, H1, J2, J3, K1, L2, L3   | Digital Video Output Port Data [0 -7] - Configurable to multiplexed 8bit, CCIR601 data formats   |
| PADDR[0] - [15]  | T2, R5, U2, U4, T4, T5, U6, U7, R9, U9, R10, T10, U11, R11, T12, R12           | External Processor Port Address [0 - 15] - Used for accessing external hardware and/or monitoring the processor activity while in debug mode                         |
| PDATA[0] - [15]  | K17, J16, J15, H17, G16, F17, G15, E16, B16, C14, A16, B14, C12, B13, C11, A11 | External Processor Port Data [0 - 15] - Used for accessing external hardware and/or monitoring the processor activity while in debug mode                            |
| READ-            | R13  | External Processor Port Read Strobe Signal   |
| WRITE-           | U14  | External Processor Port Write Strobe Signal  |
| WAIT             | U15  | External Processor Port Wait Signal - used by external devices to wait state the processor during access   |
| EXTCS[1] - [4]   | E15, D15, A10, C9  | External Chip Select [1 - 4] - Configurable device select signals  |
| FADDR[0] - [13]  | T17, P15, P16, N15, P17, N16, N17, M16, M15, M17, L14, L16, L15, L17           | Frame Memory Address [0 - 13]  |
| FADDR[14] - [23] | R16, R17<br>(FADDR16-23 N/A)   | Frame Memory Address [14 - 23]   |
| FDATA[0] - [15]  | K16, K15, J17, H16, H15, G17, F16, E17, B15, A15, C13, A14, A13, A12, B12, C10 | Frame Memory Data [0 - 15]   |
| FM_CS-           | A17  | Frame Memory Chip Select   |
| FM_CKE           | C16  | Frame Memory Clock Enable  |
| FM_CAS-          | C17  | Frame Memory Column Address Strobe   |
| FM_RAS-          | F15  | Frame Memory Row Address Strobe  |

| Pin Name       | BGA208 Pins  | Description  |
|----------------|--|--|
| FM_WR-         | B17  | Frame Memory Write   |
| GPIO[0] - [10] | A7, B7, A6, D7,<br>A5, B5, A4, B4,<br>B3, C4, A1   | General Purpose I/O [0 - 10]   |
| GPIO[11]       | D3   | General Purpose I/O [11] & Audio Codec Interface TXD Signal  |
| GPIO[12]       | C2   | General Purpose I/O [12] & Audio Codec Interface RXD Signal  |
| GPIO[13]       | C1   | General Purpose I/O [13] & Audio Codec Interface SYNC Signal   |
| GPIO[14]       | E3   | General Purpose I/O [14] & Audio Codec Interface SCLK Signal   |
| GPIO[15]       | D1   | General Purpose I/O [15] & Audio Codec Interface MCLK Signal   |
| TEST[1] - [3]  | U12, U13, T13  | Test Modes [1,2,3]<br>3=0, 2=0, 1=0 – Normal Mode<br>3=0, 2=0, 1=1 – MBIST Test Mode<br>3=0, 2=1, 1=0 – JTAG Test Mode<br>3=1, 2=1, 1=1 – SCAN Test Mode |
| MCLKI          | R14  | Main Clock Input   |
| MCLKO          | T15  | Main Clock Output  |
| MXIN           | U17  | Main Crystal Oscillator Input  |
| MXOUT          | U16  | Main Oscillator Out  |
| UXIN           | T16  | USB 48 Mhz Crystal Oscillator Input  |
| UXOUT          | R15  | USB Oscillator Out   |
| CLKDLYI        | P11  | Delayed Clock In   |
| CLKDLYO        | U10  | Delayed Clock Out  |
| SUSPEND        | T9   | Suspend Output to put external H/W in standby (Active High)  |
| RESUME         | C15  | Resume from Standby Input  |
| INT[0] - [2]   | T14, D17, D16  | External Interrupt Input [0 - 2]   |
| BUT[0] - [1]   | A3, A2   | Button Input [0 - 1]   |
| NRST           | T11  | Chip Reset - Low true  |
| VCC2V          | D8, D10, D11,<br>H4, H14, K4,<br>K14, P7, P8, P10  | Core Power 2.5VDC  |
| VCC3V          | D6, D12, F4,<br>F14, G14, L4,<br>M4, M14, P6,<br>P12                                       | I/O Power 3.3VDC   |
| VSS            | C3, D4, D5, D9,<br>D13, D14, E4,<br>E14, J4, J14, N4,<br>N14, P4, P5, P9,<br>P13, P14      | Signal/Pwr Gnd   |
| SCS0           | C8   | SPI Boot Rom Chip Select Signal  |
| SCLK           | B10  | SPI Boot Rom Clock Signal  |
| SDI            | B11  | SPI Boot Rom Data Input Signal   |
| SDO            | A9   | SPI Boot Rom Data Output Signal  |
| SCS1           | B6   | SPI Bus Chip Select 1  |
| SCS[2] - [3]   | C6, C5   | SPI Bus Chip Selects [2 - 3]   |
| TG[0] - [19]   | N2, M3, N1, P2,<br>P1, N3, R1, T1,<br>P3, R4, R3, R2,<br>U1, T3, U3, R6,<br>U5, R7, T6, R8 | Timing Generator Outputs [0 - 19]  |
| RXD            | B8   | UART Receive Data Signal   |
| TXD            | C7   | UART Transmit Data Signal  |
| RTS            | B9   | UART Request To Send   |
| CTS            | A8   | UART Clear To Send   |

| Pin Name | BGA208 Pins | Description     |
|----------|-------------|-----------------|
| USBDM    | U8          | USB Data -      |
| USBDP    | T7          | USB Data +      |
| USBPU    | T8          | USB Port Pullup |
|          | N/A         |                 |
|          |             |                 |
|          |             |                 |

### 5 ViCAM<sup>®</sup> III Electrical Specifications

ViCAM<sup>®</sup> III Digital Imaging Engine's electrical information for the BGA208 package.

#### Absolute Maximum Ratings <sup>(1)</sup>

| SYMBOL           | PARAMETER                                   | RATING                          | UNITS |
|------------------|---|---------------------------------|-------|
| V <sub>CC</sub>  | 2.5V Power Supply                           | -0.3 to 3.0                     | V     |
|                  | 3.3V Power Supply                           | -0.3 to 3.9                     | V     |
| V <sub>IN2</sub> | Input Voltage of 2.5V I/O                   | -0.3 to V <sub>CC2I</sub> + 0.3 | V     |
| V <sub>IN3</sub> | Input Voltage of 3.3V I/O with 5V Tolerance | -0.3 to 5.5                     | V     |
| T <sub>STG</sub> | Storage Temperature                         | -40 to 150                      | °C    |

#### Recommended Operating Conditions

| SYMBOL                             | PARAMETER                                   | MIN  | TYP | MAX  | UNITS |
|------------------------------------|---|------|-----|------|-------|
| V <sub>CCK</sub>                   | Core Power Supply                           | 2.25 | 2.5 | 2.75 | V     |
| V <sub>CC3O</sub>                  | Power Supply of 3.3V I/O                    | 3.0  | 3.3 | 3.6  | V     |
| V <sub>IN2</sub>                   | Input Voltage of 2.5V I/O                   | 0    | 2.5 | 2.75 | V     |
| V <sub>IN3</sub><br>T <sub>j</sub> | Input Voltage of 3.3V I/O with 5V Tolerance | 0    | 3.3 | 5.25 | V     |
|                                    | Commercial Junction Operating Temperature   | 0    | 25  | 115  | °C    |
|                                    | Industrial Junction Operating Temperature   | -40  | 25  | 125  | °C    |

#### Leakage Current and Capacitance <sup>(3)</sup>

| SYMBOL            | PARAMETER  | CONDITIONS              | MIN | TYP | MAX | UNITS |
|-------------------|--|-------------------------|-----|-----|-----|-------|
| I <sub>IL</sub>   | Input Leakage Current <sup>(2)</sup>             | No pull-up or pull-down | -10 |     | 10  | μA    |
| I <sub>OZ</sub>   | Tri-state Leakage Current                        |                         | -10 |     | 10  | μA    |
| C <sub>IN2</sub>  | Input Capacitance <sup>(3)</sup>                 |                         |     | 3.1 |     | pF    |
| C <sub>OUT2</sub> | Output Capacitance <sup>(3)</sup>                |                         |     | 3.1 |     | pF    |
| C <sub>BID2</sub> | Bi-directional Buffer Capacitance <sup>(3)</sup> |                         |     | 3.1 |     | pF    |

- (1). Permanent device damage may occur if Absolute Maximum Rating are exceeded.
- (2). The pull up/pull down input leakage current can be derived from the pull up/pull down resistance (R<sub>pu</sub>/R<sub>pd</sub>) in the DC characteristics table for each type I/O buffer.
- (3). The capacitances listed above do not include PAD capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance's which is about 0.1 pF and the package capacitance.

#### DC Characteristics of True 2.5V I/O Cells ( UXin, Uxout, MXin, MXout )

(under Recommended Operating Conditions, T<sub>j</sub> = 0°C to +115°C)

| SYMBOL                           | PARAMETER  | CONDITIONS                       | MIN                 | TYP | MAX                 | UNITS |
|----------------------------------|--|----------------------------------|---------------------|-----|---------------------|-------|
| V <sub>CCK</sub>                 | Core Power Supply                                | Core Area                        | 2.25                | 2.5 | 2.75                | V     |
| V <sub>CC2I</sub>                | Power Supply                                     | 2.5V I/O                         | 2.25                | 2.5 | 2.75                | V     |
| V <sub>CC2O</sub>                | Power Supply                                     |                                  | 2.25                | 2.5 | 2.75                | V     |
| V <sub>IL</sub>                  | Input Low Voltage                                | CMOS                             |                     |     | 0.3*V <sub>CC</sub> | V     |
| V <sub>IH</sub>                  | Input High Voltage                               | CMOS                             | 0.7*V <sub>CC</sub> |     |                     | V     |
| V <sub>t</sub>                   | Switching Threshold                              | CMOS                             |                     | 1.2 |                     | V     |
| V <sub>t-</sub>                  | Schmitt Trigger Negative Going Threshold Voltage | CMOS                             | 0.7                 | 1.0 |                     | V     |
| V <sub>t+</sub>                  | Schmitt Trigger Positive Going Threshold Voltage | CMOS                             |                     | 1.5 | 1.7                 | V     |
| V <sub>OL</sub>                  | Output Low Voltage                               | I <sub>OL</sub> =2,4,.....,16 mA |                     |     | 0.4                 | V     |
| V <sub>OH</sub>                  | Output High Voltage                              | I <sub>OH</sub> =2,4,.....,16 mA | 1.85                |     |                     | V     |
| R <sub>pu</sub> /R <sub>pd</sub> | Input Pull-up/Pull-down Resistance               |                                  | 40                  | 75  | 190                 | KΩ    |

|                 |                           |                             |     |  |    |    |
|-----------------|---------------------------|-----------------------------|-----|--|----|----|
| I <sub>IN</sub> | Input Leakage Current     | V <sub>in</sub> =0 or VCC2I | -10 |  | 10 | μA |
| I <sub>oz</sub> | Tri-state Leakage Current |                             | -10 |  | 10 | μA |

## DC Characteristics of True 3.3V I/O Cells ( USBDP, USBDN)

(under Recommended Operating Conditions, T<sub>j</sub> = 0°C to +115°C)

| SYMBOL                           | PARAMETER  | CONDITIONS                       | MIN  | TYP | MAX  | UNITS |
|----------------------------------|--|----------------------------------|------|-----|------|-------|
| V <sub>CCK</sub>                 | Core Power Supply                                | Core Area                        | 2.25 | 2.5 | 2.75 | V     |
| V <sub>CC3I</sub>                | Power Supply                                     | 3.3V I/O                         | 3.0  | 3.3 | 3.6  | V     |
| V <sub>CC3O</sub>                | Power Supply                                     |                                  | 3.0  | 3.6 | 3.6  | V     |
| V <sub>IL</sub>                  | Input Low Voltage *                              | CMOS/LVTTL                       |      |     | 0.8  | V     |
| V <sub>IH</sub>                  | Input High Voltage *                             | CMOS/LVTTL                       | 2.0  |     |      | V     |
| V <sub>t</sub>                   | Switching Threshold                              | CMOS/LVTTL                       |      | 1.5 |      | V     |
| V <sub>t-</sub>                  | Schmitt Trigger Negative Going Threshold Voltage | CMOS/LVTTL                       | 0.8  | 1.1 |      | V     |
| V <sub>t+</sub>                  | Schmitt Trigger Positive Going Threshold Voltage | CMOS/LVTTL                       |      | 1.6 | 2.0  | V     |
| V <sub>OL</sub>                  | Output Low Voltage                               | I <sub>OL</sub> =2,4,.....,16 mA |      |     | 0.4  | V     |
| V <sub>OH</sub>                  | Output High Voltage                              | I <sub>OH</sub> =2,4,.....,16 mA | 2.4  |     |      | V     |
| R <sub>pu</sub> /R <sub>pd</sub> | Input Pull-up/Pull-down Resistance               |                                  | 40   | 75  | 190  | KΩ    |
| I <sub>IN</sub>                  | Input Leakage Current                            | V <sub>in</sub> =0 or VCC3I      | -10  |     | 10   | μA    |
| I <sub>oz</sub>                  | Tri-state Output Leakage Current                 |                                  | -10  |     | 10   | μA    |

\* The input level is CMOS and LVTTL compatible. The V<sub>il(max)</sub> = 0.3V<sub>CC</sub> of CMOS also complied with the V<sub>il(max)</sub> = 0.8 for LVTTL spec. The V<sub>ih(min)</sub> = 2V of LVTTL also complied with the V<sub>ih(min)</sub> = 0.7\*V<sub>CC</sub>

## DC Characteristics of 5V Tolerant 3.3V Programmable I/O Cells

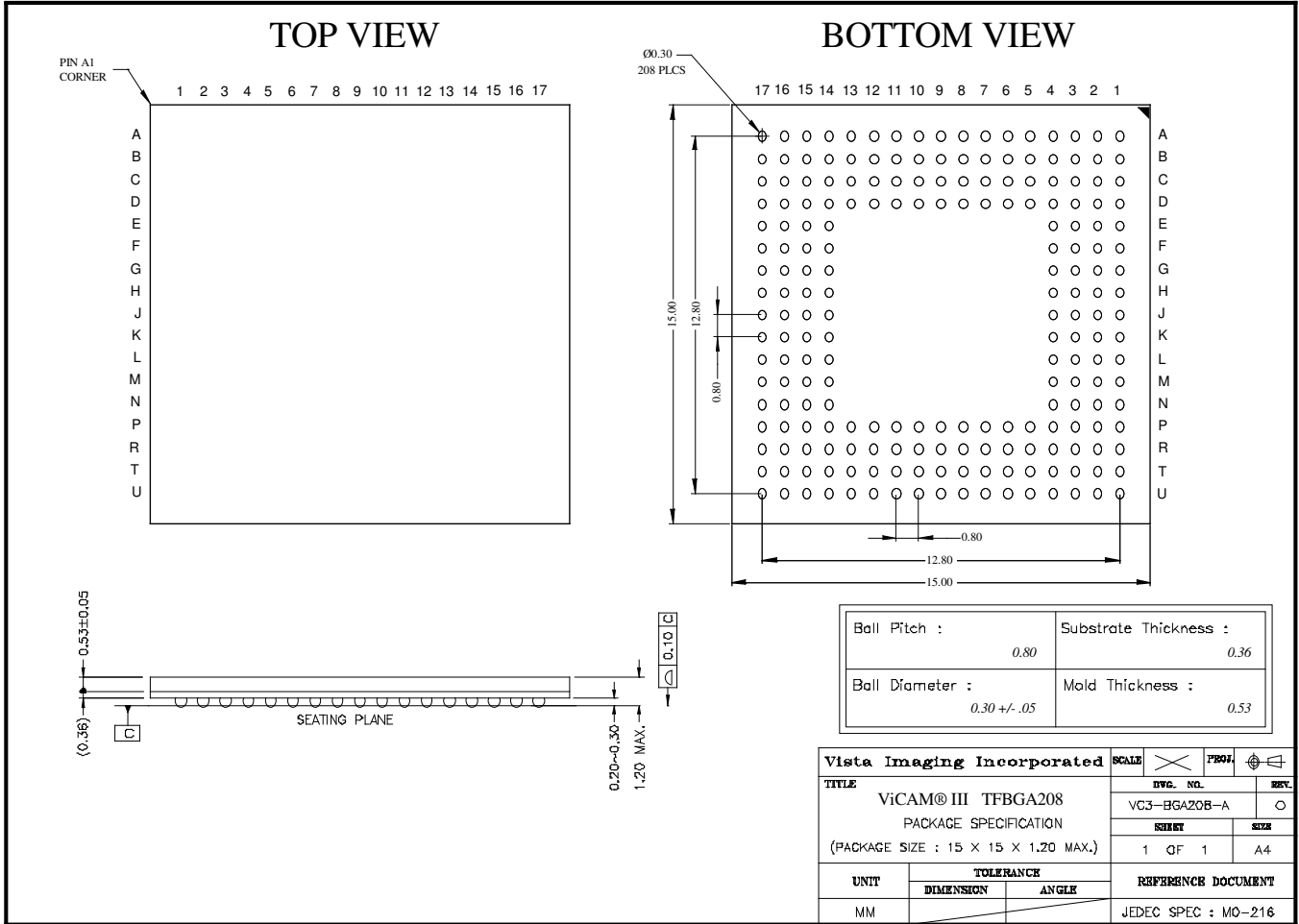
(under Recommended Operating Conditions, T<sub>j</sub> = 0°C to +115°C)

| SYMBOL                           | PARAMETER                          | CONDITIONS                  | MIN                 | TYP | MAX                 | UNITS |
|----------------------------------|------------------------------------|-----------------------------|---------------------|-----|---------------------|-------|
| V <sub>CCK</sub>                 | Core Power Supply                  | Core Area                   | 2.25                | 2.5 | 2.75                | V     |
| V <sub>CC3I</sub>                | Power Supply                       | 3.3V I/O                    | 3.0                 | 3.3 | 3.6                 | V     |
| V <sub>CC3O</sub>                | Power Supply                       |                             | 3.0                 | 3.3 | 3.6                 | V     |
| V <sub>IL</sub>                  | Input Low Voltage                  | PCI                         | -0.5                |     | 0.3*V <sub>cc</sub> | V     |
| V <sub>IH</sub>                  | Input High Voltage                 |                             | 0.5*V <sub>cc</sub> |     | 5.5                 | V     |
| V <sub>t</sub>                   | Switching Threshold                | PCI                         |                     | 1.3 |                     | V     |
| V <sub>OL</sub>                  | Output Low Voltage                 | I <sub>OUT</sub> = 1.5 mA   |                     |     | 0.1*V <sub>cc</sub> | V     |
| V <sub>OH</sub>                  | Output High Voltage                | I <sub>OUT</sub> = 0.5 mA   | 0.9*V <sub>cc</sub> |     |                     | V     |
| R <sub>pu</sub> /R <sub>pd</sub> | Input Pull-up/Pull-down Resistance |                             | 40                  | 75  | 190                 | KΩ    |
| I <sub>IN</sub>                  | Input Leakage Current              | V <sub>in</sub> =0 or VCC3I | -10                 |     | 10                  | μA    |
| I <sub>oz</sub>                  | Tri-state Output Leakage Current   |                             | -10                 |     | 10                  | μA    |

Vista Imaging assumes no responsibility for usage beyond the conditions within this specification.

### 6 ViCAM<sup>®</sup> III Package Information

This section presents the details of the ViCAM<sup>®</sup> III Digital Imaging Engine's package information for the BGA208 package.



VC3-B208-A Package Drawing

### 7 ViCAM<sup>®</sup> III Soldering Reflow Instructions

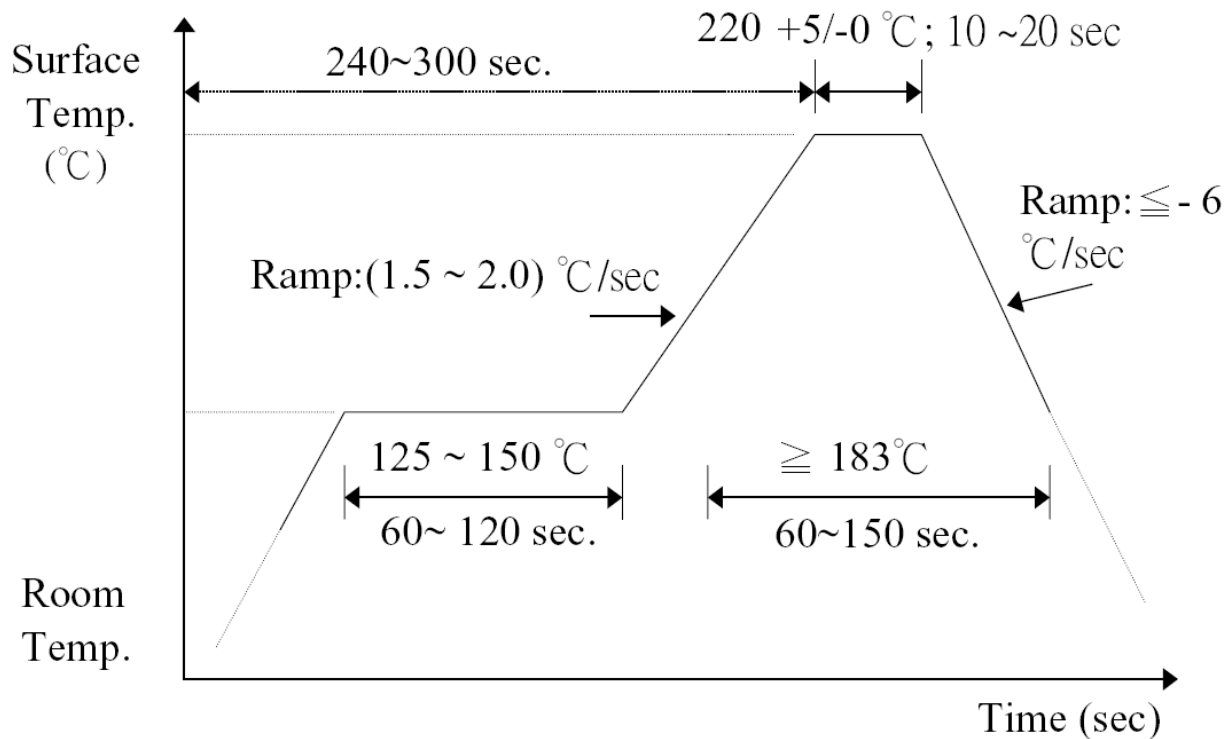
**Package Reflow Condition:**

- Convection 220 +5/-0 °C
- VPR 215~ 219 °C
- IR / Convection 220 +5/-0 °C

**Reflow Profile:**

|                                       | Convection or IR / Convection | VPR                 |
|---------------------------------------|-------------------------------|---------------------|
| Average ramp-up rate (183 °C to Peak) | 3 °C / second max.            | 10 °C / second max. |
| Preheat temp 125 (+25) °C             | 120 seconds max.              |                     |
| Temp maintained above 183 °C          | 60 ~ 150 seconds              |                     |
| Time within 5 °C of actual peak temp  | 10 ~ 20 seconds               | 60 seconds          |
| Peak temperature range                | 220 +5 / -0 °C                | 215 ~ 219 °C        |
| Ramp-down rate                        | 6 °C / second max.            | 10 °C / second max. |
| Time 25 °C to peak temp               | 6 minutes max.                |                     |

**Note:** All temperatures refer to the top side of the package, measured on the package body surface. The devices shall be allowed to cool down for five minutes minimum between Convection, IR/Convection, or VPR cycles.



### 8 ViCAM<sup>®</sup> III Ordering Information

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| Part Number | Package                   |
|-------------|---------------------------|
| VC3-B208-A  | 208 pin BGA (15mm x 15mm) |

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